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Grid Voltage Synchronization by using the technique of Series Compensation

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Abstract: series capacitors are used to reduce the voltage drop in the lines with low power factor and improve the voltage at the receiving end especially with LPF loads. Series compensation is nothing but an insertion of reactive power elements into transmission lines and provides the following benefits such as reduced voltage drops, increased system response, Good stability and High efficiency. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algorithms, which are able to work under unbalanced and distorted conditions. The proposed project analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three- phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency- locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. The simulation results are presented by using Mat lab/Simulink software.

Keywords: Grid Voltage, Synchronization, Micro Grid ,Series Compensation.

I. INTRODUCTION

A micro grid is a part of distribution network that includes multiple loads and distributed energy resource converters thatare operated in parallel with the boarder utility grid [1]. It helps in integration of distributed energy resource converters to micro grid. Micro grid is a part of distributed generation system. It is a localized grouping of electricity generation, energy storage and a load that normally operates connected toa traditional centralized utility grid. The component of micro grid involves distributed generation resources such as photovoltaic panels, small wind turbines, fuel cells, etc. The storage devices are batteries, super capacitors, flywheel etc along with local loads. Better efficiency, superior quality with high reliability of power supply having environmental aswell as economical benefits can be achieved by using microgrid [2]. A droop control is a control technique applied to distributed generation system for primary frequency control and as well as voltage control for load sharing between local loads to utility Grid. By controlling the frequency, as well as voltage, corresponding active power
(P) and reactive power (Q) can be controlled in distributed generation. Increase in active power output results in reduction of frequency and the corresponding increase in the reactive power results in decrease of voltage as explained in [3]. The concept of Phase Locked Loop (PLL) is used for the implementation of grid synchronization method. PLL is used for the estimation of grid voltage, phase angle and frequency. A PLL is a control system in which output signalis generated by relating its phase to the phase of an input signal. A PLL can track an input frequency or it can generate a frequency that is a multiple of the input frequency as explained in [4]. This paper a series compensation controller based synchronization method is proposed for achieving the grid synchronization in terms of frequency, phase angle, amplitude of output voltages, active power and reactive power in between converter output and Distributed Energy Resource Converters (DERCs). The series compensation controller is replaced by proportional integral (PI) controller for obtaining fast dynamic response, low steady error and for stable operation [8].

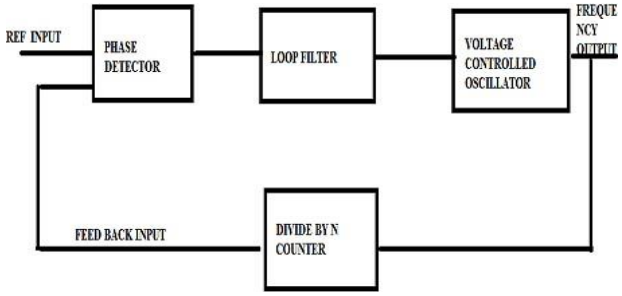

Fig.1. Block Diagram of PLL Controller.

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The primary controller senses the difference voltage from the utility grid voltage and point of common coupling voltage. A phase locked loop block is used in the primary controller to generate the input frequency signals from the primary controller. A phase locked loop is a control loop which generates an output signal by comparing its phase to the phase of an input signal. By maintaining the input and output frequencies lock step also implies keeping the input and output frequencies the same. It can also sense a frequency, in addition of synchronizing the signals [9-10]. The concept on series compensation set theory was introduced by L. A. Zadeh in 1965. Series compensation is rule based and it is application of human knowledge on system behavior as explained in. Fig.2 represents theschematic diagram of series compensation based system.

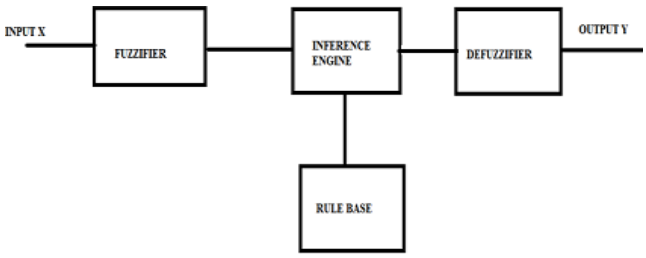

Fig.2. Schematic of Series Compensation Based System

Series compensation controller operation mainly involves theexecution of four major operations:

- Fuzzification
- Rule based Inference system
- Composition and De fuzzification

Fuzzification involves the conversion of crisp values or classical set values to Series compensation rule base values. It involves the choice of Variables, series compensation Input and output variables and the evaluation of membership functions. It involves series compensation subset rules, composition and de fuzzification. For assigning each series compensation subset rule based value to the output variable a Rule based series compensation inference system is necessary. Composition helps in forming a Single series compensation subset rule based Value assigned to an output variable from a multiple rule based seriescompensation subset values. De fuzzification helps in theconversion of composition of series compensation rule based value to a single crisp value [11-12]. De fuzzification helps in the conversion of composition of seriescompensation rule based value to a single crisp value. API controller is replaced with a series compensation controlleris as shown in fig.3. The main objective of designing the Series compensation logic rules is to synchronize the grid parameters such as grid frequency, phase angle, amplitude of output voltages, active power and reactive power with the output of the distributed energy resource converters. The error and change of error are the inputs of the series compensation controller.

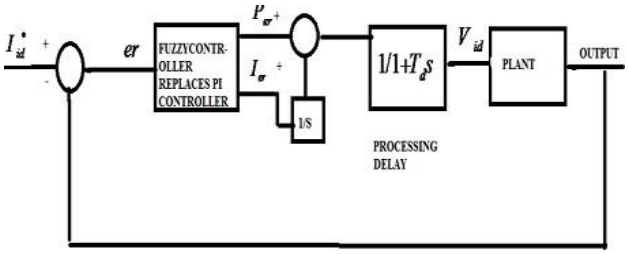

Fig.3. Block Diagram of Series Compensation Controller

II. GRID SYNCHRONIZATION ECIFICATIONSBASED ON GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on analyzing the individual dynamic performance of each proposal, without first determining a time response window within the dynamic behavior of the system under test, whichwould be considered to be satisfactory. In this paper, in order to evaluate the response of the grid synchronization topologies under test, a common performance requirement for all the structures has been established in this section, considering the needs that can be derived from the LVRT requirements. Despite the fact that the detection of the fault can be carried out with simpler algorithms, as shown in and,the importance of advanced grid synchronization systems lies in the necessity

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of having accurate information aboutthe magnitude and phase of the grid voltage during the fault,in order to inject the reactive power required by the TSO .In the German standard [2], it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the generator transformer to at least 2% of the rated current for each percent of the voltage dip, as shown in Fig.4. 100% reactive power delivery must be possible, if necessary.

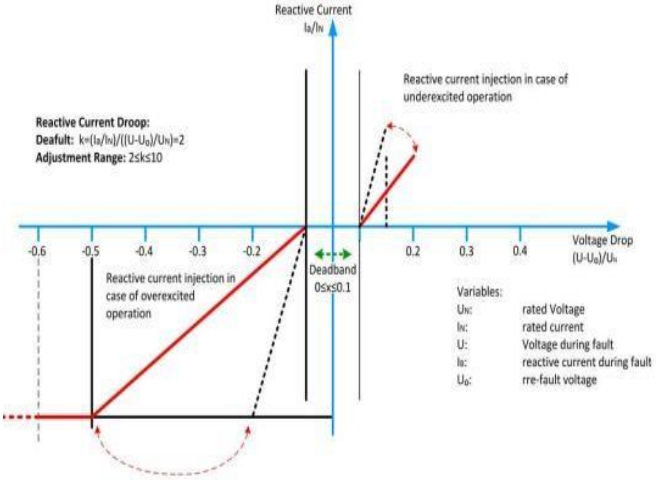

Fig.4. E-on Voltage Support Requirement in the Eventof Grid Fault.

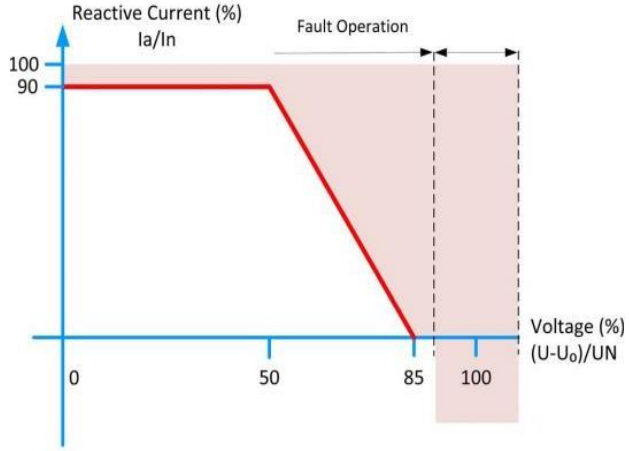

Fig.5. REE Voltage Support Requirement in the Eventof Grid Fault.

A similar condition is given in the Spanish grid code,where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop andbe able to inject full reactive power after 150 ms, as shown inFig.5. Considering these demands, this paper will consider that the estimation of the voltage conditions will be carried out within20–25 ms, as this target permits it to fulfill themost restrictive requirements, in terms of dynamical response, available in the grid codes. This condition will be extended to frequency estimation; although this parameter is more related to secondary control algorithms than LVRT, the same time window between20 and 25 ms will be considered in this work for the detection of the disturbance.

III. DESCRIPTION OF THE THREESYNCHRONIZATION SYSTEMS

Many of the positive-sequence detection algorithms arebased on SRF PLLs. Despite having a good response underbalanced conditions, their performance becomesinsufficient in unbalanced faulty grids (95% of cases), and their good operation is highly conditioned to the frequency stability, which is in compatible with the idea of a robust synchronization system.

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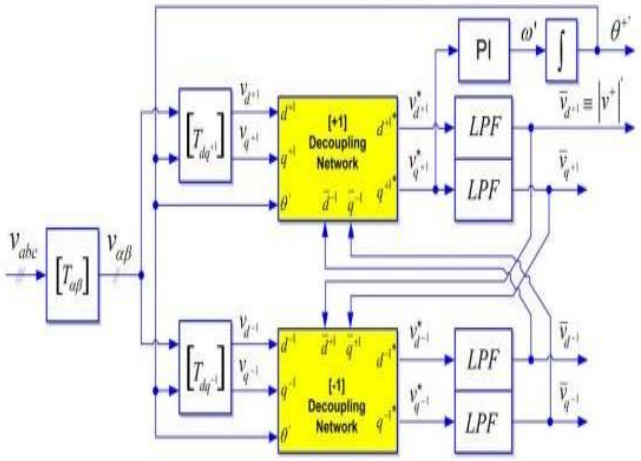

Fig.6. DDSRF-PLL Block Diagram.

Many authors have discussed different advanced models, which are able to overcome the problems of the classical PLL, using frequency and amplitude adaptive structures which are able to deal with unbalanced, faulty, and harmonic-polluted grids. In the framework of these topologies, three PLL structures will be discussed and evaluated in this paper.

A. DDSRF PLL

The DDSRF PLL published in and was developed forimproving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counterclockwise and another one clockwise, in order to achieve an accurate detection of the positive- and negative-sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF PLL is shown in Fig.6. When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a dcvoltage on the dq+1 axes of the positive-sequence SRF and as a voltages at twice the fundamental utility frequency on the dq−1axes of the negative-sequence SRF. In contrast, thenegative sequence voltage vector will cause a dc componenton the negative-sequence SRF and an ac oscillation on the positive sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches the dclevel on the negative sequence SRF and vice versa, a decoupling network is applied to signals on the d-q positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters (LPFs) inFig.6 are responsible for extracting the dc component from the signal on the decoupled SRF axes. These dc components collect information about the amplitude and phase angle of thepositive- and negative-sequence components of the grid voltage vector. Finally, the PI controller of the DDSRF PLLworks on the decoupled q-axis signal of the positive- sequence SRF (v∗q+1)and performs the same function as in an SRF PLL, aligning the positive-sequence voltage with the d-axis. This signal is free of ac components due to the effect of the decoupling networks; the bandwidth of the loopcontroller can be consequently increased.

B. DSOGI PLL

The operating principle of the DSOGI PLL for estimatingthe positive- and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the αβ stationary reference frame, as explained. The diagram of the DSOGI PLL is shown in Fig.7. As it can be noticed, the ISC methodis implemented by the positive-sequence calculation block. To apply the ISC method, it is necessary to have a set of signals, *vα–vβ*, representing the input voltage vector on the *αβ* stationary reference frame together with another set of signals, *qvα–qvβ*, which are in quadrature and lagged with respect to *vα–vβ*. In the DSOGI PLL, the signals to besupplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI), which is an adaptive band pass filter based on the generalized integrator concept. At its output, the DSOGI provides four signals, namely, *vα* and *vβ*, which are filtered versions of *vα* and *vβ*, respectively, and *qvα and qvβ,* which are the in-quadrature versions of *vα* and *vβ*.

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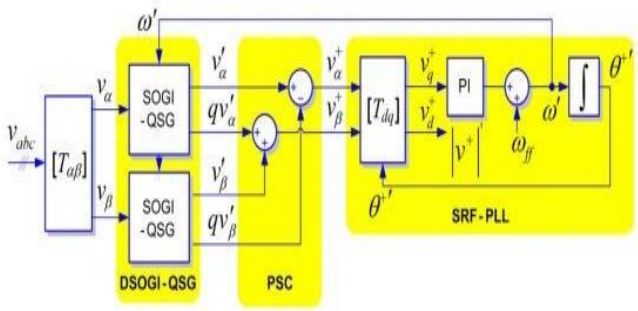

Fig.7. DSOGI-PLL Block Diagram.

A conventional SRF PLL is applied on the estimatedpositive-sequence voltage vector, $v\alpha\beta$ +, to make this synchronization system frequency adaptive. In particular,the $v\alpha\beta$ + voltage vector is translated to the rotating SRF, and the signal on the q-axis, $v+q$, is applied at the input of theloop controller. As a consequence, the fundamental grid frequency (ω) and the phase angle of the positive-sequence voltage vector ($\theta+$) are estimated by this loop. The estimated frequency for the fundamental grid component is fed back to adapt the center frequency ω of the DSOGI.

C. 3phEPLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has proven to provide good results in single phase synchronization systems. An EPLL is essentially an adaptive band pass filter, which is able to adjust the cut off frequency as a function of the input signal. Its structure was later adapted for the three-phase case, in order to detect the positive-sequence vector of three-phase signals, obtaining the 3phEPLL that is represented in Fig.8.In this case, each phase voltage is processed independentlyby an EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency
,vn and j_{vn}, the second one being 90◦ with respect to vn. The resulting signals constitute the input for the computational unit. Owing to these in-quadrature signals, the instantaneous positive-sequence voltage component, $v_{abc}+$, can be estimatedby means of using the ISC method.

IV. DISCRETE IMPLEMENTATION

The performance of the different structures under test is really dependent on their final digital implementation, particularly on the discretization approach made to their continuous equations. This implementation is critical and should be studied in detail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL. Some methods, such as the forward Euler, the backward Euler, and the Tustin(trapezoidal) numerical integration, off area goodperformance when used for discrediting other synchronization systems. However, Euler methods can beinadequate under certain conditions, due to the need of introducing additional sample delays. Therefore, according tothe specific needs of the presented topologies, this section will describe the discrete representation of each PLL individually. In order to facilitate the comprehension of the process, the different building blocks that appear at Figs. 6–8 will be referenced.

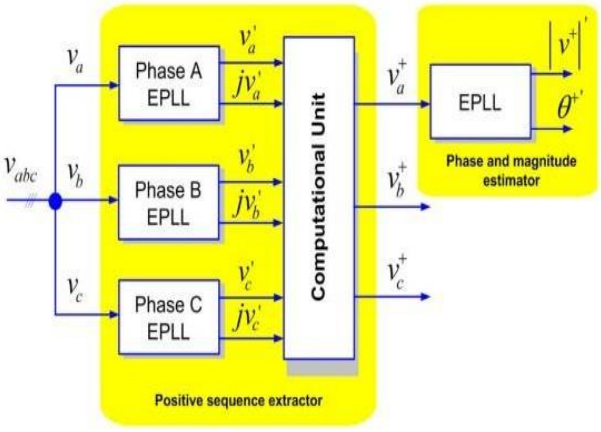

Fig.8. 3phepll Block Diagram.

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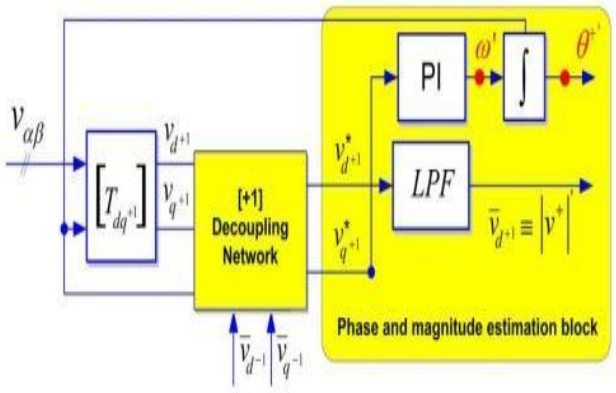

Fig.9. Phase and Magnitude Estimation Loop of the DDSRF PLL.

A. DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained since the continuous representation of several parts does notchange in the discrete domain. This is the case for the transformation blocks Tαβ, Tdq+1, and Tdq−1, whose description can be found, in general, scope literature.

1. Positive and Negative-Sequence Decoupling Networks

The decoupling network constitutes one of the most important contributions of this synchronization method. Thediscrete equations of these blocks are shown in (1), being almost the same as in the continuous domain. It is justnecessary to consider one sample delay of θ, $v\bar{}d{-}1$, $v\bar{}q{-}1$, $v\bar{}d{+}1$, and $v\bar{}q{+}1$ in order to avoid algebraic loops.

2. Phase and Magnitude Estimator Discretization

In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 9). However, this does not affect the discretization of the phase and magnitude estimator since v∗d+1 and vq∗+1 act as the input of this block

$$\begin{bmatrix} v^*_{d+1}[n+1] \\ v^*_{q+1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d-1}[n] \\ \bar{v}_{q-1}[n] \end{bmatrix}$$

$$\times \begin{bmatrix} v^*_{d-1}[n+1] \\ v^*_{q-1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d-1}[n+1] \\ v_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d+1}[n] \\ \bar{v}_{q+1}[n] \end{bmatrix} \quad (1)$$

The discrete controller and the integrator can be built usinga backward numerical approximation. The frequency and phase can then be represented in the z-domain (2),considering v∗q+1as the error to be minimized. In this equation, a feed forward of the nominal frequency is given by means of ωff.

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q+1}(z) + \omega_{ff}$$

$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

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Finally, sample-based representation gives rise to hare theexpressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q+1}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1] \quad (3)$$

In these equations, a frequency feed forward has beenintroduced as an initial condition to ω'.

3. LPF Block Discretization

The amplitudes of the dq positive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse responses (IIR) LPFs extract the ripple from each sequence estimation in order to reinforcethe performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency ωf , equal to half of the grid frequency, was originally proposed in; hence, the same transfer function has been implemented in this paper forevaluation purposes in

$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$
$$x[n+1] = y[n]. \quad (4)$$

B. DSOGI-PLL Discretization

1. DSOGI-QSG Block Discretization: As was previously mentioned, the DSOGI-based quadrature signal generator (QSG) of Fig.10 consists of two independent and decoupled second-order generalized integrators (SOGIs).Therefore; eachSOGI-based quadrature signal generator can be discredited individually, thus facilitating it's mathematical description. InFig.10, the block diagram of the implemented SOGI is shown.

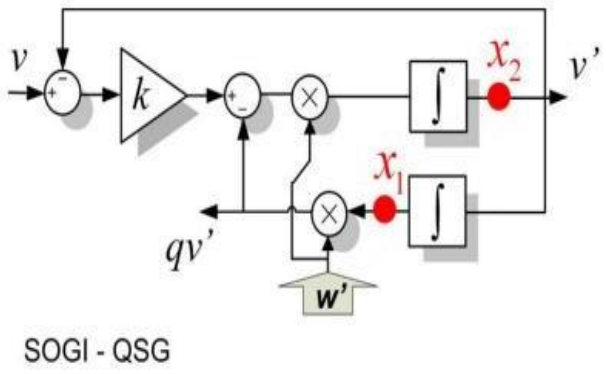

Fig.10. Quadrature Signal Generator Based on a SecondOrder Generalized Integrator (SOGI QSG).

This quadrature signal generator (QSG) is a linear system itself; therefore, a discrete representation can be systematically obtained if the continuous state space is previously deducted. The equations of the SOGI state space appear detailed in (5).where v constitutes the input while v and qv are the two in quadrature output signals

$$\left.\begin{aligned} \dot{x}_n &= A \cdot x_n + B \cdot v \\ y_n &= C \cdot x_n \end{aligned}\right\}; \quad x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \; y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix}$$
$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k \cdot \omega' \end{bmatrix} \; B = \begin{bmatrix} 0 \\ k \cdot \omega' \end{bmatrix} \; C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix}$$

(5)

$$A' = \gamma \begin{bmatrix} 4 + 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 & 4T_s \\ -4T_s \cdot \omega'[n]^2 & 4 - 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 \end{bmatrix}, \; B' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ 4k \cdot \omega'[n] \end{bmatrix}$$
$$C' = \gamma \begin{bmatrix} -2T_s^2 \cdot \omega'[n]^2 & 4T_s \\ 2T_s \cdot \omega'[n] \cdot (2 + T_s \cdot k \cdot \omega'[n]) & 2T_s^2 \cdot \omega'[n] \end{bmatrix}, \; D' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ k \cdot T_s^2 \cdot \omega'[n]^2 \end{bmatrix}$$
$$\gamma = \frac{1}{4 + 2 \cdot T_s \cdot k \cdot \omega'[n] + T_s^2 \cdot \omega'[n]^2}$$

(6)

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The discretization of this system has been performed using trapezoidal integrators, as they offer a better detection of thephase, which is important when dealing with sinusoidal signal. The symbolic values of each matrix of (7) are detailed in (6), shown at the bottom of the page. In these matrices, Ts is the sampling time of the discrete system, ω'[n] is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and k is the SOGI gain

$$x[n+1] = A' \cdot x[n] + B' \cdot v[n]$$
$$y[n] = C' \cdot x[n] + D' \cdot v[n]. \quad (7)$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure Where Ts is the sampling time. The resultingdiscrete system is the best option as it reduces the need of using additional delays for breaking algebraic loops thatappear using other methods which do not consider the SOGIQSG as a whole.

$$A' = \left(I + \frac{A \cdot T_s}{2}\right)\left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$B' = \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot B$$
$$C' = T_s \cdot C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$D' = C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot \frac{B \cdot T_s}{2} \quad (8)$$

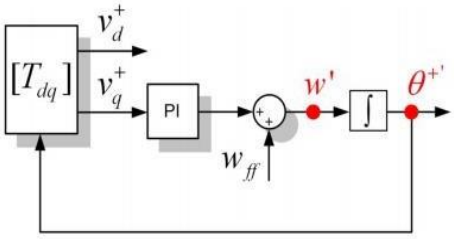

Fig.11. State Variables of the SRF-PLL Block.

2. SRF PLL Discretization: The frequency and phase detection is obtained by means of the SRF PLL shown in Fig.11. The discretization of the controller and the integrator is performed using the backward numerical approximation. The frequency and phase can then be represented in the z- domain, as shown in (9), where v+q constitutes the error to be minimized

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V_{q+1}^*(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (9)$$

It can be noticed that the previous equations in (9) are equal to (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample-based representation of (9) can be written as shown in

$$\omega'[n+1] = \omega'[n] - k_p \cdot v_{q+1}^*[n] + (k_p + k_i \cdot T_s) \cdot v_{q+1}^*[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1] \quad (10)$$

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phasevoltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

3. QSG Block—EPLL Discretization: The block diagramof the EPLL implemented in this paper is presented in Fig.12.

$$v'[n+1] = A'[n+1] \cdot \cos(\theta'[n+1]) \quad (13)$$

This type$qv'[n+1] = -A'[n+1] \cdot \sin(\theta'[n+1])$ accurate tuning, due to the fact that the stable regions of the s-plane and z-plane are different. However, its major simplicity,compared to the Tustin or backward integration, benefits from the computational speed of this block.

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4. Computational Block Unit: The description for this block is the same in both discrete and continuous domains. Nevertheless, specific equations are used in this paper, as shown in (14).

5. Phase and Magnitude Detection Block: This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the Positive-sequence fundamental component. Its discretization is equal to that shown in (12).

$$\begin{aligned} v_b^+[n] &= -\left(v_a^+[n] + v_c^+[n]\right) \\ v_a^+[n] &= \frac{1}{3}v'_a[n] - \frac{1}{6}(v'_b[n] + v'_c[n]) + \frac{1}{2\sqrt{3}}(jv'[n]_b - jv'_c[n]) \\ v_c^+[n] &= \frac{1}{3}v'[n]_c - \frac{1}{6}(v'_a[n] - v'_b[n]) + \frac{1}{2\sqrt{3}}(jv'_a[n] - jv'_b[n]) \end{aligned} \tag{14}$$

V. SERIES COMPENSATION

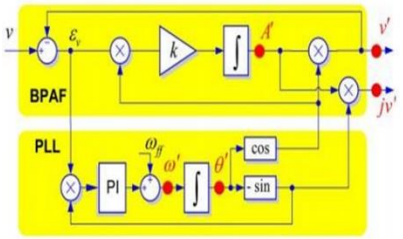


Fig.12. Quadrature Signal Generator Based on an EPLL Structure

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$\begin{aligned} \dot{A}'(t) &= k \cdot e(t) \cdot \cos\theta'(t) \\ \dot{\omega}'(t) &= -k_i \cdot e(t) \cdot \sin\theta'(t) \\ \dot{\theta}(t) &= \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t). \end{aligned} \tag{11}$$

The discrete state space variable representation using a forward Euler approximation to reach satisfactory results; therefore, the same method has been implemented here.

$$\begin{aligned} e[n+1] &= u[n+1] - v'[n] \\ A'[n+1] &= A'[n] + T_s \cdot k \cdot e[n] \cdot \cos(\theta'[n]) \\ \omega'[n+1] &= \omega'[n] - T_s \cdot k_i \cdot e[n] \cdot \sin(\theta'[n]) \\ \theta'[n+1] &= \theta'[n] + T_s \cdot \omega'[n] - T_s \cdot k_p \cdot e[n] \cdot \sin(\theta'[n]) \end{aligned} \tag{12}$$

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadraturesignals

Series Compensation Method A dynamic voltage restorer(DVR) was introduced for mitigating a voltage sag. The DVR is based on an Voltage source converter (VSC) systemthat has energy storage for supplying active power, an output filter to make output voltage wave sinusoidal, and a step up transformer connected in series with line. A DVR is configured as a series-connected voltage controller. To control the output voltage of the DVR, the inverter supplies the missing load voltage using self-commutable electronic switches such as a gate turn-off thyristor (GTO), or an insulated gate bipolar transistor (IGBT), or an insulated gatecommutated thyristor (IGCT). A DVR injects the missing voltage in series; it can be called a series voltage controller, but the term DVR is commonly used now. The advantages of the DVR are fast response, ability to compensate for voltage sag and a

voltage phase shift using an inverter system. Three schemes can be used to generate the missing voltage in series with the source voltage for compensating the voltage sag such as, In-phase voltage injection

- Phase-invariant voltage injection
- Phase advanced voltage injection
- In the in-phase voltage injection scheme,

The injecting voltage has the same phase angle of the source voltage. Therefore, the magnitude of the injected voltage is the smallest among three compensation schemes. However, this scheme requires the largest active power. In case of the phase invariant voltage injection scheme, the DVR injects the missing voltage that keeps the magnitude of the voltage as well as the phase of the supply voltage. This scheme needs a large injected voltage and may cause over injection of reactive power. Since the size of energystorage is closely related to the requirement of active power, various compensation methods to reduce the requirement of active energy have been proposed. If the injected voltage is inquadrature with the load current, the DVR does not inject active power. This scheme is highly dependent on the load power factor and may generate a sudden jump of the voltage phase angle. To avoid sudden phase angle jump, the phase of the injected voltage should be gradually changed at the beginning of the compensation as well as at the restoration in order not to disturb the operation of sensitive loads. The high-speed PWM switching and output filter makes it possible to achieve a fast response with less harmonic distortion. However, DVR are expensive because of the converter systems, the inserting transformer, and energy storages to supply active and reactive power for the missing voltage.

VI. MATLAB/SIMULATION RESULTS

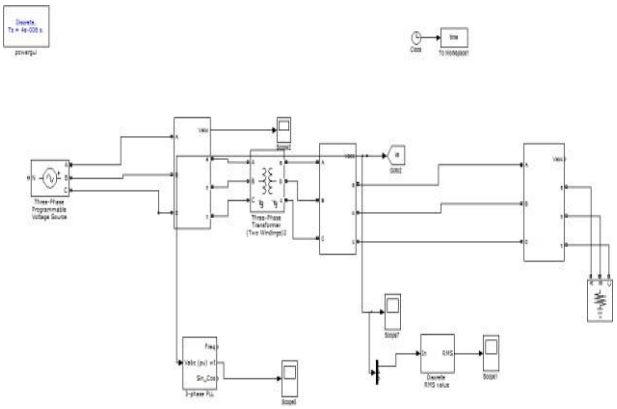
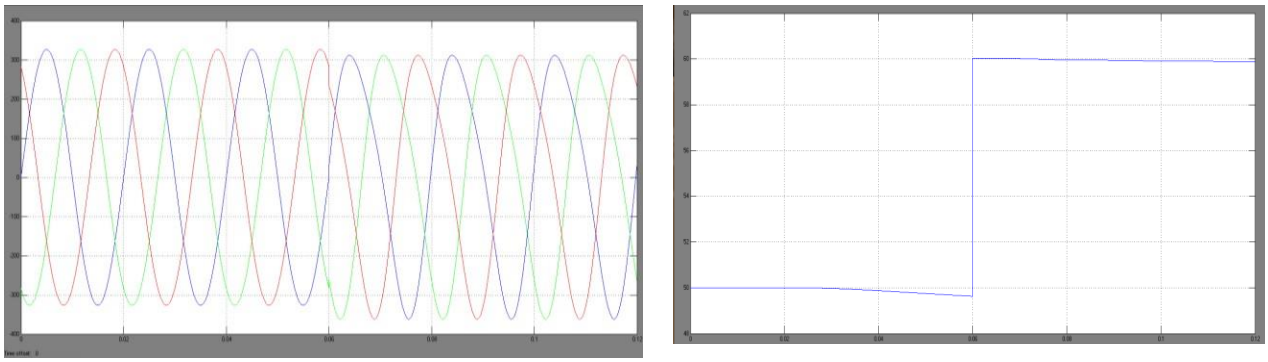


Fig.13. Matlab/Simulation Circuit of Decoupled Double Synchronous Reference Frame PLL (DDSRF PLL)



(a) **(b)**

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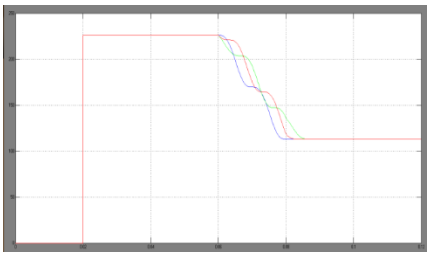


(c)

Fig.14. Simulation Wave Form DDSRF Harmonic,Frequency, LLLG and Unbalance Condition

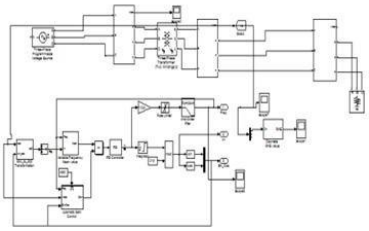
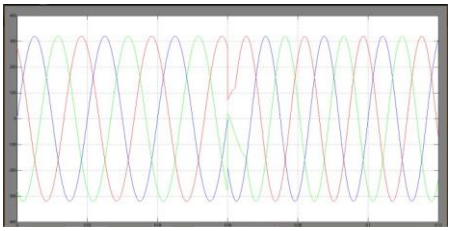
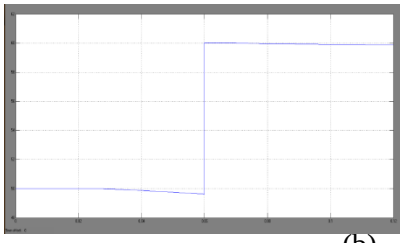


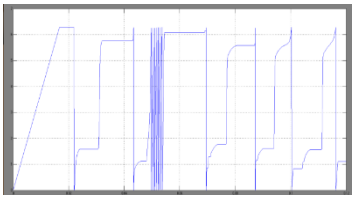
Fig.15. Matlab/Simulation Circuit of Dual Second OrderGeneralized Integrator PLL



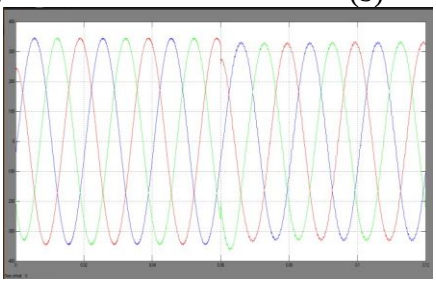
(a)



(b)



(c)



(d)

Fig.16. Simulation Wave Form DSOGPLL Harmonic,Frequency, LLLG and Unbalance Condition

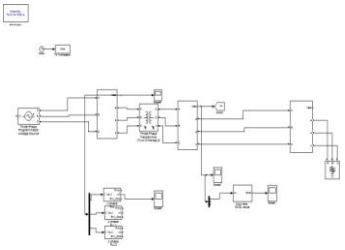


Fig.17.Matlab/Simulation Circuit of Three-PhaseEnhanced PLL (3phepll).

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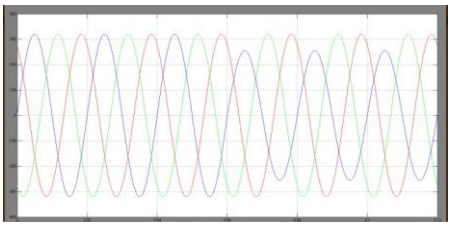
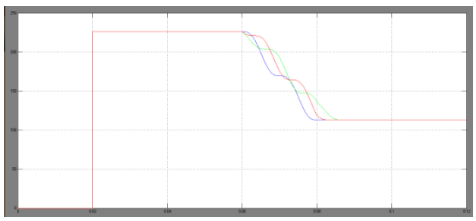
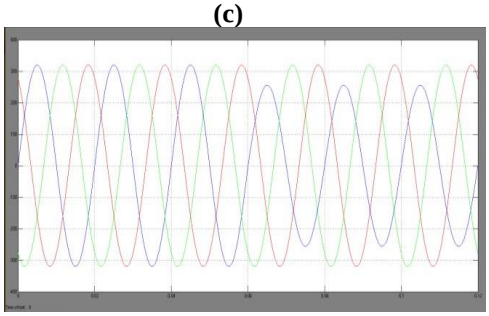
(a)



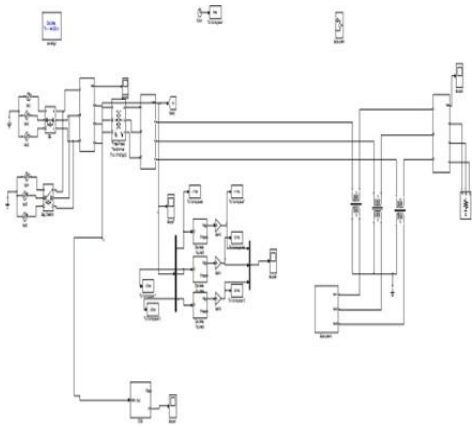


(c)



(d)

Fig.18. Simulation Wave Form of (3phepll)



Harmonic, frequency, LLLG and unbalance condition

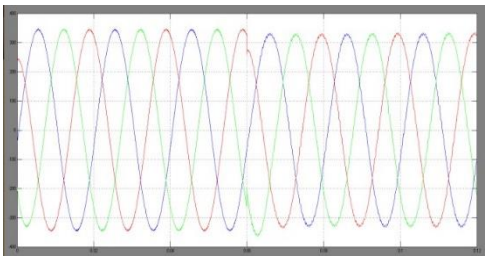
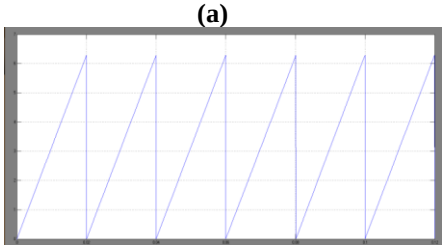
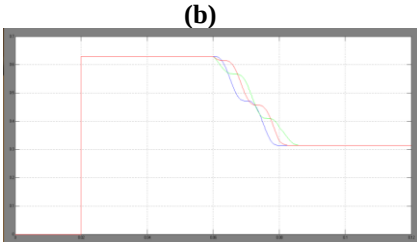


Fig.19. Matlab/ Simulation Circuit of Series Compensation

(a)



(b)



(c)

Fig.20. Simulation Wave Form of Series CompensationHarmonic, frequency, LLLG and unbalance condition.

VII. CONCLUSION

This paper developed a Series compensation based Grid voltage Synchronization for Distributed Generated System. A series compensation based secondary controller is used for achieving the grid synchronization by integrating the distributed energy resource converters to micro grid. The simulation results with series compensation controller helpsin obtaining the quick response, low steady state error and reduces the harmonics with low ripple content. The power factor is also improved near PCC and power quality has been increased by the influence of multiple types of DG sources in distribution generation system. Hence, the proposed series compensation system has better performance for achieving grid synchronization. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing thecomputational burden, as compared to the 3phEPLL, without affecting its performance.

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